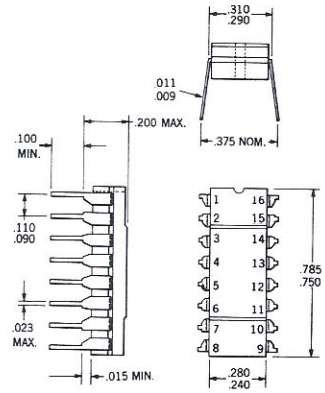
9304
MSI DUAL FULL ADDER
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9304 consists of two independent, high speed, binary full adders. The adders are useful in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion, and majority gating. The circuit uses TTμL for high speed, high fanout operation and is compatible with all members of the CCSL group of digital integrated circuits.

- **Multi-function capability**
- **8ns carry propagation delay**
- **Complementary inputs and outputs available**
- **Typical power dissipation of 150 mW**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL and TTμL families (CCSL).**
- **All ceramic "HERMETIC" 16-pin Dual In-Line* package**
- **Input clamp diodes limit high speed termination effects**

PHYSICAL DIMENSIONS



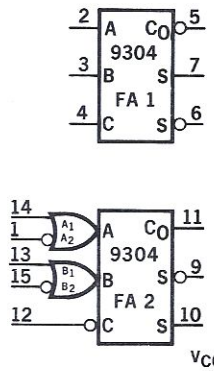
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Fig. 1

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Fig. 2

ORDER INFORMATION

Specify U6B9304XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

*Fairchild patent pending

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MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

FUNCTIONAL DESCRIPTION

The Fairchild 9304 logic block consists of two separate high speed carry dependent sum full adders. This design allows a minimum carry propagation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active high or active low inputs at the A and B terminals. The adders produce a low carry and both low and high sum with active high inputs, a high carry and both high and low sum when active low inputs are used. This principle of duality is shown in Figure 12, where the adders are drawn as functional blocks.

The Truth Table and Loading Rules for the 9304 are shown in Table I and Table II.

TABLE I — TRUTH TABLES

ADDER 1					
INPUTS			OUTPUTS		
C	B	A	$\overline{C}_O$	$\overline{S}$	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

ADDER 2							
INPUTS					OUTPUTS		
$\overline{C}$	B_1	A_1	$\overline{B}_2$	$\overline{A}_2$	C_O	S	$\overline{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

H = High Voltage Level
L = Low Voltage Level

TABLE II —

LOADING RULES (1 U.L. = TTμL Gate Input Unit Load)

INPUTS		LOADING
FA 1	A, B & C	4 U.L.
FA 2	$\overline{A}_2$, $\overline{B}_2$ & $\overline{C}$	4 U.L.
	A_1 & B_1	1 U.L.

OUTPUTS		FANOUT
FA 1	$\overline{C}_O$	7 U.L.
	$\overline{S}$	9 U.L.
	S	10 U.L.
FA 2	C_O	7 U.L.
	S	9 U.L.
	$\overline{S}$	10 U.L.

TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B930451X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2$ mA (Pins 7 & 9) $V_{CC} = 4.5\ V$, $I_{OH} = -1.08$ mA (Pins 6 & 10) $V_{CC} = 4.5\ V$, $I_{OH} = -0.84$ mA (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 16$ mA (Pins 7 & 9) $I_{OL} = 14.4$ mA (Pins 6 & 10) $I_{OL} = 11.2$ mA (Pins 5 & 11) $V_{CC} = 4.5\ V$, $I_{OL} = 12.4$ mA (Pins 7 & 9) $I_{OL} = 11.2$ mA (Pins 6 & 10) $I_{OL} = 8.7$ mA (Pins 5 & 11)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$4\ I_F$	Input Load Current		−6.4		−4.4	−6.4		−6.4		
I_F	Input Load Current		−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$4\ I_F$	Input Load Current		−4.96		−3.88	−4.96		−4.96		
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
$4\ I_R$	Input Leakage Current				60	240		240		Ground on other inputs
t_{pd+}	C to C_O				8	13			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Fig. 11
t_{pd-}	C to C_O				8	13			ns	
t_{pd+}	A_i to $\overline{S}$				28	40			ns	
t_{pd-}	A_i to $\overline{S}$				25	35			ns	

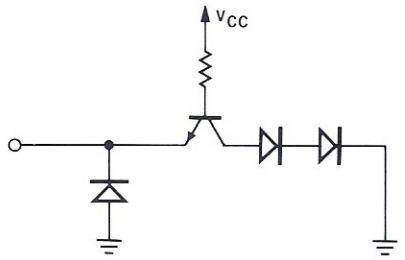
TABLE IV —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part #U6B930459X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2$ mA (Pins 7 & 9) $V_{CC} = 4.75\ V$, $I_{OH} = -1.08$ mA (Pins 6 & 10) $V_{CC} = 4.75\ V$, $I_{OH} = -0.84$ mA (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16$ mA (Pins 7 & 9) $I_{OL} = 14.4$ mA (Pins 6 & 10) $I_{OL} = 11.2$ mA (Pins 5 & 11) $V_{CC} = 4.75\ V$, $I_{OL} = 14.1$ mA (Pins 7 & 9) $I_{OL} = 12.7$ mA (Pins 6 & 10) $I_{OL} = 9.85$ mA (Pins 5 & 11)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
$4\ I_F$	Input Load Current		−6.4		−4.0	−6.4		−6.4		
I_F	Input Load Current		−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
$4\ I_F$	Input Load Current		−5.64		−3.6	−5.64		−5.64		
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
$4\ I_R$	Input Leakage Current				60	240		240		Ground on other inputs
t_{pd+}	C to C_O				8.0	15			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Fig. 11
t_{pd-}	C to C_O				8.0	15			ns	
t_{pd+}	A_i to $\overline{S}$				28	45			ns	
t_{pd-}	A_i to $\overline{S}$				25	40			ns	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS

EQUIVALENT CIRCUIT



INPUT CURRENT VS INPUT VOLTAGE

FIG. 3 PINS 1, 2, 3, 4, 12, 15

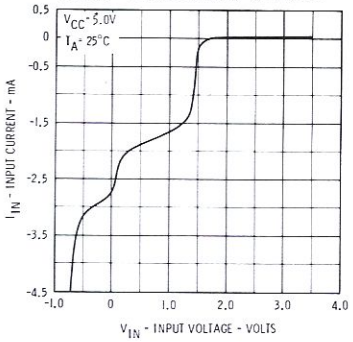
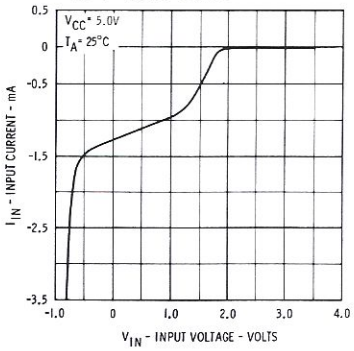
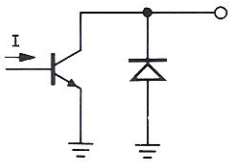


FIG. 4 PINS 13, 14

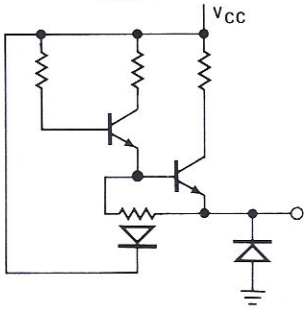


OUTPUTS

LOW STATE



HIGH STATE



OUTPUT CURRENT VS OUTPUT VOLTAGE

FIG. 5 LOW STATE

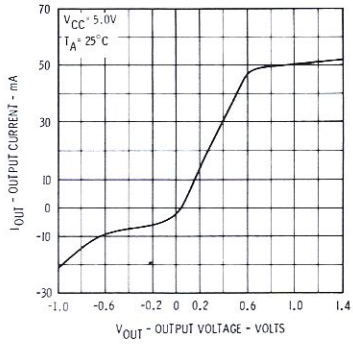


FIG. 6 HIGH STATE

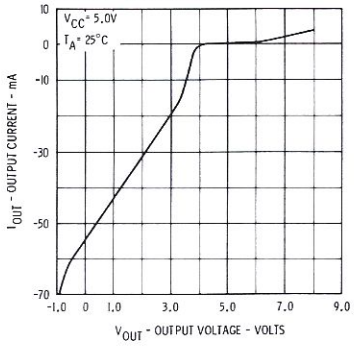


Fig. 7
TYPICAL CARRY TURN ON DELAY TIME VERSUS TEMPERATURE

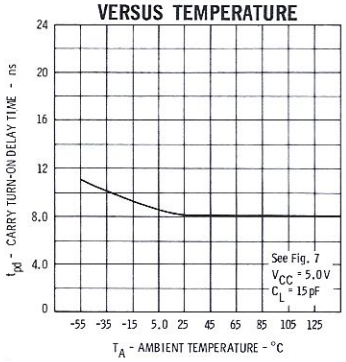


Fig. 8
TYPICAL CARRY TURN OFF DELAY TIME VERSUS TEMPERATURE

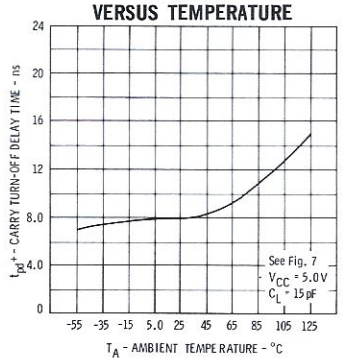


Fig. 9
TYPICAL ADD TURN ON DELAY TIME VERSUS TEMPERATURE

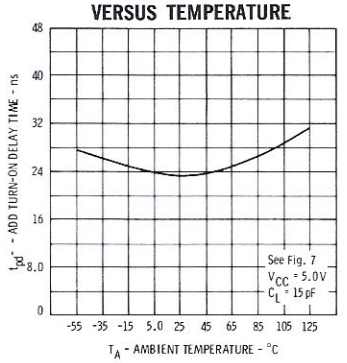
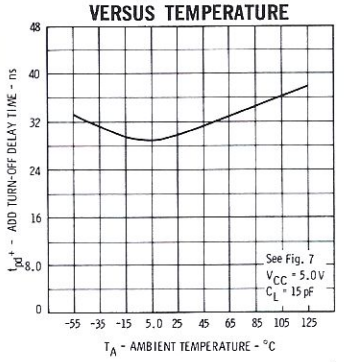
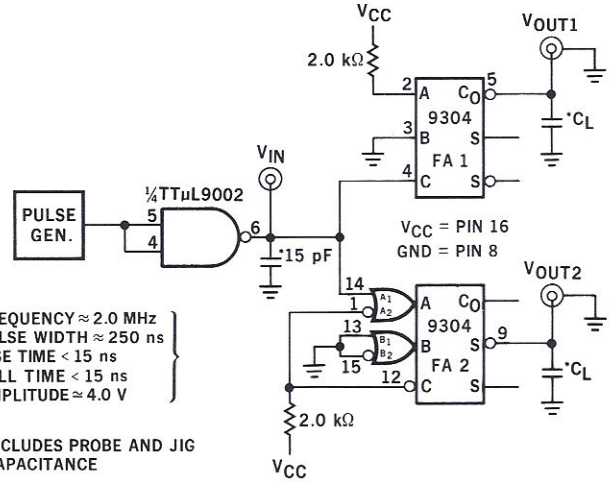


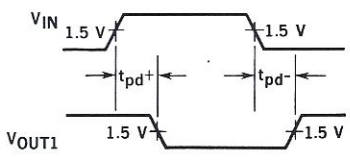
Fig. 10
TYPICAL ADD TURN OFF DELAY TIME VERSUS TEMPERATURE





FREQUENCY ≈ 2.0 MHz
PULSE WIDTH ≈ 250 ns
RISE TIME < 15 ns
FALL TIME < 15 ns
AMPLITUDE ≈ 4.0 V

*INCLUDES PROBE AND JIG CAPACITANCE



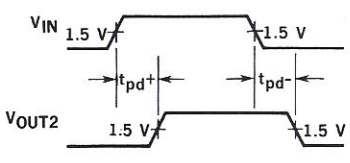


Fig.11— SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

APPLICATIONS — The 9304 dual adder has been designed to be useful in a wide variety of applications such as addition, parity generation and checking, code conversion, majority gating and other applications for which this combination of logic gates may be useful. The multifunctional capabilities of the Fairchild dual adder can be seen from reference to the applications shown.

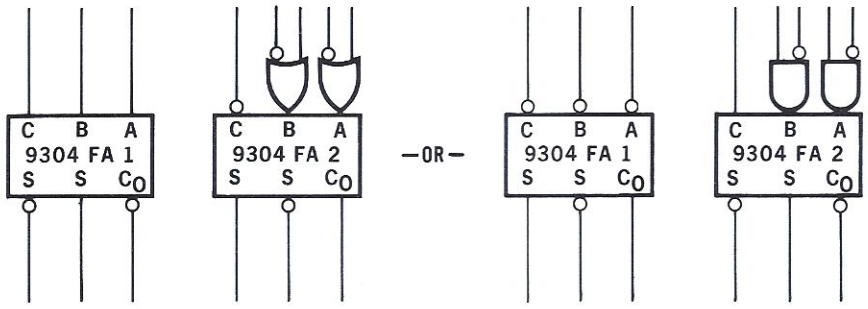


Fig.12— FUNCTIONAL BLOCK REPRESENTATION

The principle of duality allows 2 ways of representing each adder. The circuit is the same in both cases but the logic diagrams differ. The dual diagrams facilitate logic design and allow a greater understanding of the capabilities of the device.

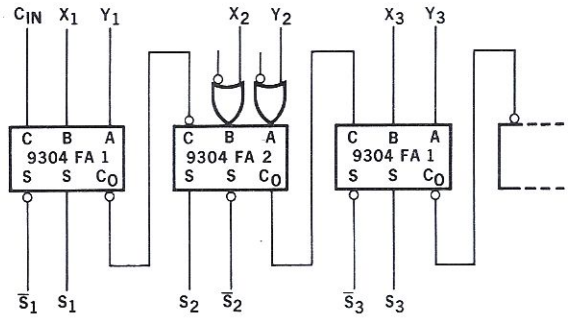


Fig.13— RIPPLE CARRY PARALLEL ADDITION

Shown above is a high speed ripple carry parallel addition scheme. Only one and-or-not gate relay is incurred at each stage allowing a typical addition speed of (N+1) x 8 ns, where N is the number of bits in the word. A similar scheme will work if the negation inputs are used, and the design acts as a subtractor when the complement of one variable is provided.

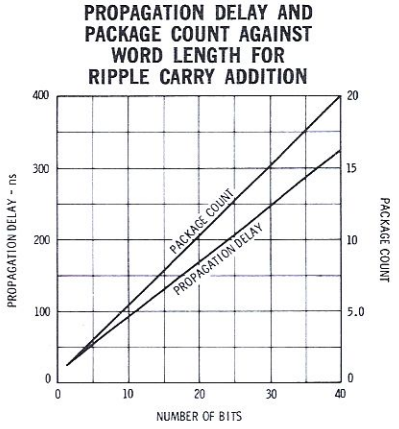


Fig. 14

The curve shows propagation delay of the ripple Carry Adder drawn in Figure 5. Plotted on the same diagram is a curve showing the low package count resulting from this Ripple Scheme.

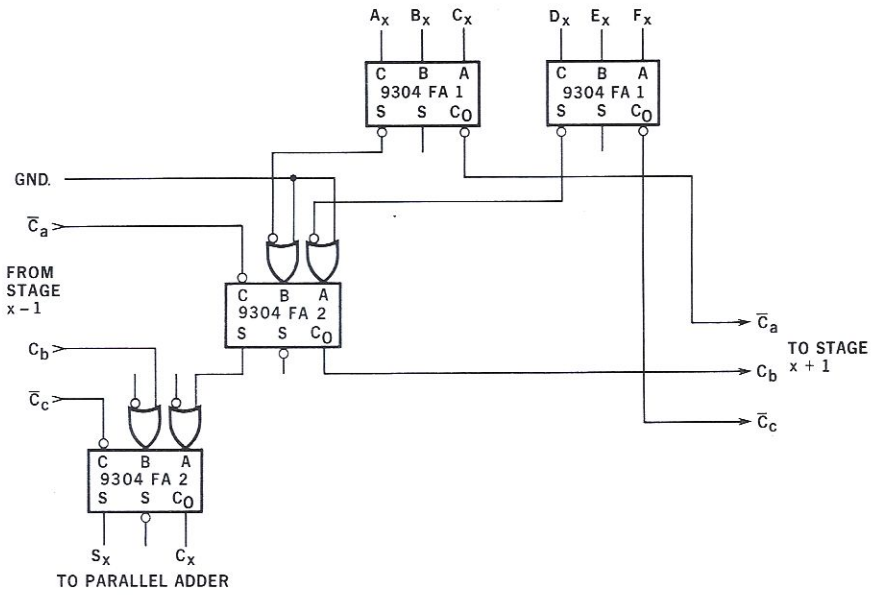


Fig. 15 — ADDITION OF SIX VARIABLES

The above design shows how the 9304 can be used in carry save arithmetic. Six input variable are reduced to two where they can be added in a parallel adder. Delay between inputs and outputs is typically 50 ns, allowing extremely high speed computation. Additional variables may be added or the concept can be extended to multiplication, division, and various other arithmetic operations.

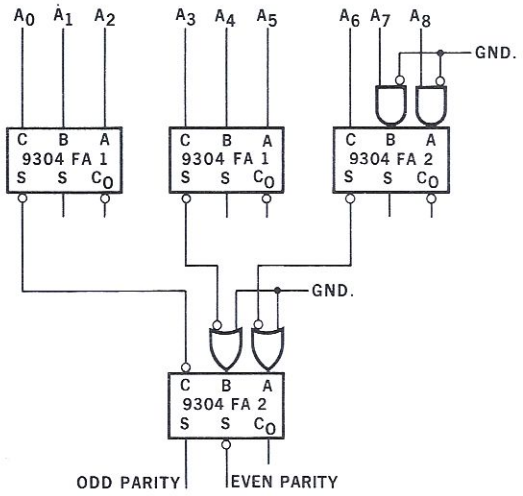


Fig. 16 — BYTE PARITY GENERATION OR CHECKING

The 9304 can be used for parity checking or generating. The above design uses 2 9304's to generate parity for an 8 bit byte or check parity over 9 bits. The delay from input to odd parity is typically 35 ns. Additional adder blocks can be used to generate or check parity over larger word lengths. The concept can also be used for hamming and cyclic code generation and checking.

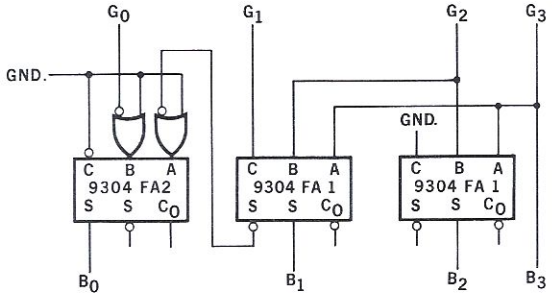


Fig. 17 — 4 BIT PARALLEL GRAY TO BINARY CONVERSION

A 4 bit parallel binary to gray conversion is shown. The adders can also be used for other cyclic code manipulations.

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